ABSTRACT OF THE DISCLOSURE

A clock generation circuit capable of generating a high-frequency clock with a simple circuit configuration, together with a data transfer control device and an electronic instrument using the same. The clock generation circuit has: serially-connected inversion circuits IV0 to IV4 in which an output of IV4 is connected to an input of IV0 by a feedback line FL; and buffer circuits BF0 to BF4 which receives outputs from IV0 to IV4. The inversion circuits IV0 to IV4 are disposed along a line LN1 and the buffer circuits BF0 to BF4 are disposed along a line LN2 that is parallel to the feedback line FL but different from LN1. Dummy lines DL0 to DL3 each of which having parasitic capacitance that is equal to that of the feedback line FL are connected to the inversion circuits IV0 to IV3, to equalize the phase differences between clocks CK0 to CK4. The feedback line FL and the dummy lines DL0 to DL3 are disposed in a region between the inversion circuits IV0 to IV4 and the buffer circuits BF0 to BF4. Between which edges of multi-phase clocks an edge of data (data transferred in USB 2.0 HS mode) is located is detected, and a clock selected on the basis of edge detection information is set as a sampling clock.